# A 0.5 μm SILICON BIPOLAR TRANSISTOR FOR LOW PHASE NOISE OSCILLATOR APPLICATIONS UP TO 20 GHz

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## ABSTRACT

An interdigitated silicon bipolar transistor with 0.5 micrometer emitter width and 2 micrometer emitter-emitter pitch has been fabricated which has a measured Fmax greater than 30 GHz. Low phase noise YIG-tuned oscillators with fundamental frequency bands of 4-18 and 8-22 GHz have been demonstrated using this transistor.

## INTRODUCTION

The effects of lateral scaling on the high frequency performance of small-signal silicon bipolar transistors are well known. The associated gain is maximized by increasing the ratio of the emitter periphery to the base area and decreasing the base resistance. This can be accomplished by scaling down the emitter width and reducing the emitter-emitter pitch in an inderdigitated transistor design (1,2). The theoretical maximum frequency of oscillation, Fmax, at which the maximum available gain is unity will likewise increase.

## DEVICE PROCESS AND DESIGN

Using thick local oxide isolation, ion implantation, dry etching and self-aligning submicrometer photolithography, arsenic emitter silicon bipolar transistors with 0.5 micrometer emitter width and 2.0 micrometer emitter-emitter pitch have been successfully fabricated. This aggressive scaling represents more than a factor of two reduction in the critical emitter-emitter pitch compared to previously reported fine-geometry bipolar transistors (1,2).

Three different sized transistor, AT210, AT220 and AT240, were designed with 10, 20 and 40 emitters respectively. The length of the emitters were 10 micrometers for the AT210 and 15 micrometers for the AT220 and AT240. A photograph is shown in Fig. 1 of the three transistors which were fabricated on a single 13 X 13 mil die.

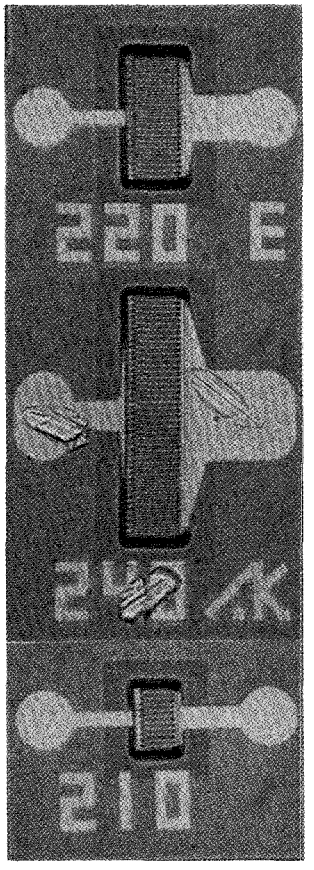


FIG. 1. THREE 0.5 MICROMETER SILICON BIPOLAR TRANSISTOR DESIGNS: AT210, AT220 AND AT240 (MAGNIFIED 1600X).

The small-signal T-equivalent circuit shown in Fig. 2 was successful in modeling the transistor S-parameters at frequencies up to Ku band. The appropriate element values for the AT220 biased at Vce = 10 V and Ie = 20 mA are listed in Table 1. The total base-collector capacitance is less than .07 pF and the small-signal base resistance is less than 7 ohms.



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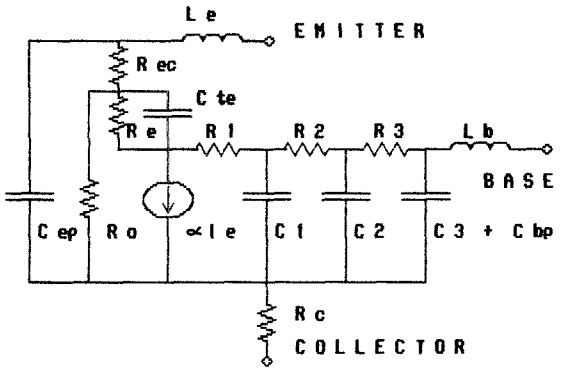



FIG. 2. SMALL-SIGNAL BIPOLAR TRANSISTOR EQUIVALENT CIRCUIT

TABLE 1: SMALL-SIGNAL BIPOLAR TRANSISTOR EQUIVALENT CIRCUIT ELEMENT VALUES FOR AT220 BIASED AT Vce = 10 V, Ie = 20 mA.

| | | |
|---|---|---|
| Le | EMITTER BOND WIRE INDUCTANCE | 0.10 nH |
| Lb | BASE BOND WIRE INDUCTANCE | 0.15 nH |
| Cep | EMITTER BOND PAD CAPACITANCE | 0.015 pF |
| Cbp | BASE BOND PAD CAPACITANCE | 0.008 pF |
| Rec | EMITTER CONTACT RESISTANCE | 0.2 ohms |
| Rbc | BASE CONTACT RESISTANCE | 1.0 ohms |
| Ro | EARLY EFFECT RESISTANCE | 1000 ohms |
| Rc | COLLECTOR RESISTANCE | 4.0 ohms |
| R1 | DISTRIBUTED BASE RESISTANCE | 2.1 ohms |
| R2 | | 2.4 ohms |
| R3 | | 1.0 ohms |
| C1 | DISTRIBUTED BASE CAPACITANCE | 0.016 pF |
| C2 | | 0.017 pF |
| C3 | | 0.023 pF |
| Re | kT/qI AT Ie = 20 mA | 1.3 ohms |
| Cte | EMITTER-BASE JUNCTION CAPACITANCE | 2.0 pF |

$\alpha \quad (\alpha_o/(1+F/Fb))EXP(-j2\pi F\tau d)$

Fb = 25 GHz

$\tau d$ = 7 psec

## DEVICE PERFORMANCE

S-parameter measurements were made with the transistors die attached onto a 15 mil thick ceramic chip carrier and bonded in a common emitter configuration using 0.7 mil Au wire. Typical results are listed in Table 2 for an AT220 biased at Vce = 10 V and Ie = 20 mA. The Ft was 10 GHz and Fs where S21 = 0 dB was also approximately 10 GHz. Maximum Available Gain (MAG) was 21.8 dB at 2 GHz and 15.7 dB at 4 GHz. Maximum Unilateral Gain (MUG) was 6 dB at 18 GHz.

TABLE 2: S-PARAMETERS FOR THE AT220 MOUNTED ON A CHIP CARRIER AND BIASED AT Vce = 10 V, Ie = 20 mA.

| F | S11 | | S21 | | S12 | | S22 | |
|---|---|---|---|---|---|---|---|---|
| GHz | mag | ang | dB | ang | mag | ang | mag | ang |
| 1 | .67 | -160 | 20.0 | 100 | .018 | 40 | .61 | -27 |
| 2 | .71 | 178 | 14.4 | 78 | .022 | 46 | .57 | -34 |
| 4 | .73 | 158 | 8.4 | 52 | .034 | 60 | .60 | -51 |
| 6 | .75 | 142 | 4.6 | 31 | .048 | 66 | .65 | -68 |
| 9 | .77 | 127 | 0.8 | 6 | .080 | 68 | .73 | -86 |
| 12 | .81 | 111 | -2.0 | -14 | .130 | 65 | .77 | -100 |
| 15 | .84 | 97 | -3.3 | -35 | .160 | 40 | .77 | -120 |
| 18 | .94 | 84 | -7.0 | -55 | .200 | 35 | .78 | -144 |

When S21 and MAG are plotted against frequency (Fig. 3), it is evident that a 2 dB improvement in gain has been achieved compared to the AT414, a high-performance commercially available transistor with an emitter-emitter pitch of 4 micrometers. Extrapolating the MAG of the AT220 to unity gain indicates an Fmax in excess of 30 GHz. The Fmax of the intrinsic AT220 is estimated to be about 40 GHz if chip carrier parasitics and bond wire parasitic inductances are accounted for.

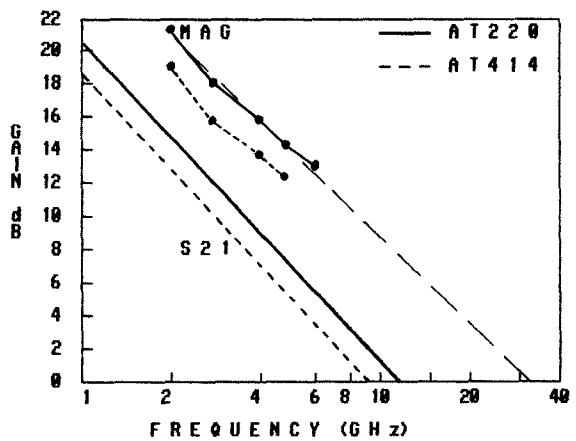



FIG. 3. S21 AND MAG VERSUS FREQUENCY OF 2 MICROMETER EMITTER-EMITTER PITCH AT220 COMPARED TO THE 4 MICROMETER PITCH AT414.

## APPLICATION IN YIG-TUNED OSCILLATORS

Interest in using silicon bipolar transistors rather than GaAs FETs for oscillator applications arises from their wide negative resistance bandwidth and their fundamentally lower and more reproducible 1/f noise characteristics. Lower 1/f noise leads directly to lower phase noise for equal loaded resonator Q in YIG, varactor and cavity tuned oscillators.

Wideband YIG oscillators have generally employed silicon bipolar transistors for frequencies up to 12 GHz and GaAs FETs for frequencies from 8 to 50 GHz. Doubling-circuit techniques have been used successfully in hyperabrupt varactor tuned oscillators to cover the 6.9 to 19.2 GHz band with bipolar transistors (3). However, this approach requires a much more complex MIC circuit and has significantly higher phase noise than the higher Q YIG tuned oscillator.

To exploit the higher Fmax and lower 1/f noise of the AT200 transistors, Ku band YIG tuned MIC oscillators with GaAs MMIC buffer amplifiers (4) were designed and fabricated. A simplified schematic of the YIG oscillator circuit is shown in Fig. 4. It was found that the widest tuning bandwidths could be achieved with the AT220 whereas the AT240 delivered approximated 3 dB more power with a 20 % reduction in the maximum frequency of oscillation.

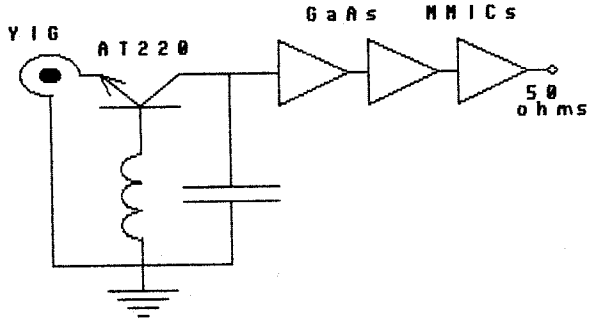
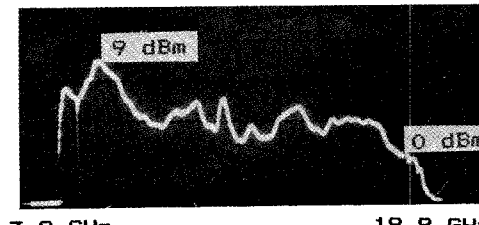
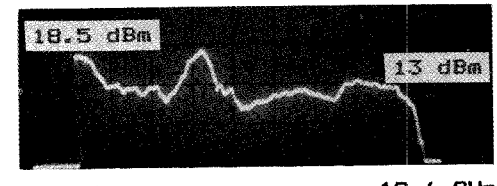



FIG. 4. SIMPLIFIED SCHEMATIC OF BIPOLAR TRANSISTOR BASED YIG-TUNED OSCILLATOR WITH GaAs MMIC BUFFER AMPLIFIERS.

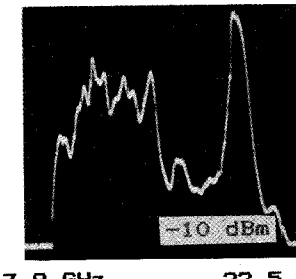
The swept oscillator output signals with and without the MMIC buffer amplifiers are shown in Fig. 5(a) and 5(b) for a design optimized for the 4 to 18 band. The unbuffered output power varied from 9 dBm at 4.5 GHz to 0 dBm at 18 GHz. The addition of the three GaAs MMIC distributed buffer amplifiers increased the output power to 18.5 dBm at 4 GHz and 13 dBm at 18 GHz. The swept output signal for a design optimized for the 8 to 22 GHz band is shown in Fig. 5(c).




3.9 GHz (a) 18.9 GHz




3.6 GHz (b) 18.6 GHz




7.8 GHz (c) 22.5 GHz

FIG. 5. OUTPUT OF YIG-TUNNED OSCILLATORS USING THE AT220 SILICON BIPOLAR TRANSISTOR.
(a) 4 - 18 GHz UNBUFFERED
(b) 4 - 18 GHz GaAs MMIC BUFFERED
(c) 8 - 22 GHz UNBUFFERED

The measured oscillator single-sideband phase noise normalized to a 1 Hz bandwidth at 20 kHz from the carrier is shown in Fig. 6 over the 4 to 18 GHz band for the AT220 bipolar transistor and over the 8 to 18 GHz band for a typical GaAs FET fabricated on vapor-phase epi. The bipolar based YIG oscillator covers a one octave larger bandwidth and is approximately 10 dB quieter then the FET based version.

Although lower phase noise has been occasionally observed with vapor phase epi GaAs FETs, the bipolar transistor provides low phase noise with much greater consistency. The bipolar transistor YIG oscillators are also observed to have fewer spurious signals over the -54 to 100 C military temperature range. In addition they show promise of eventually enabling the entire 2 to 20 GHz band to be covered with a single YIG oscillator.

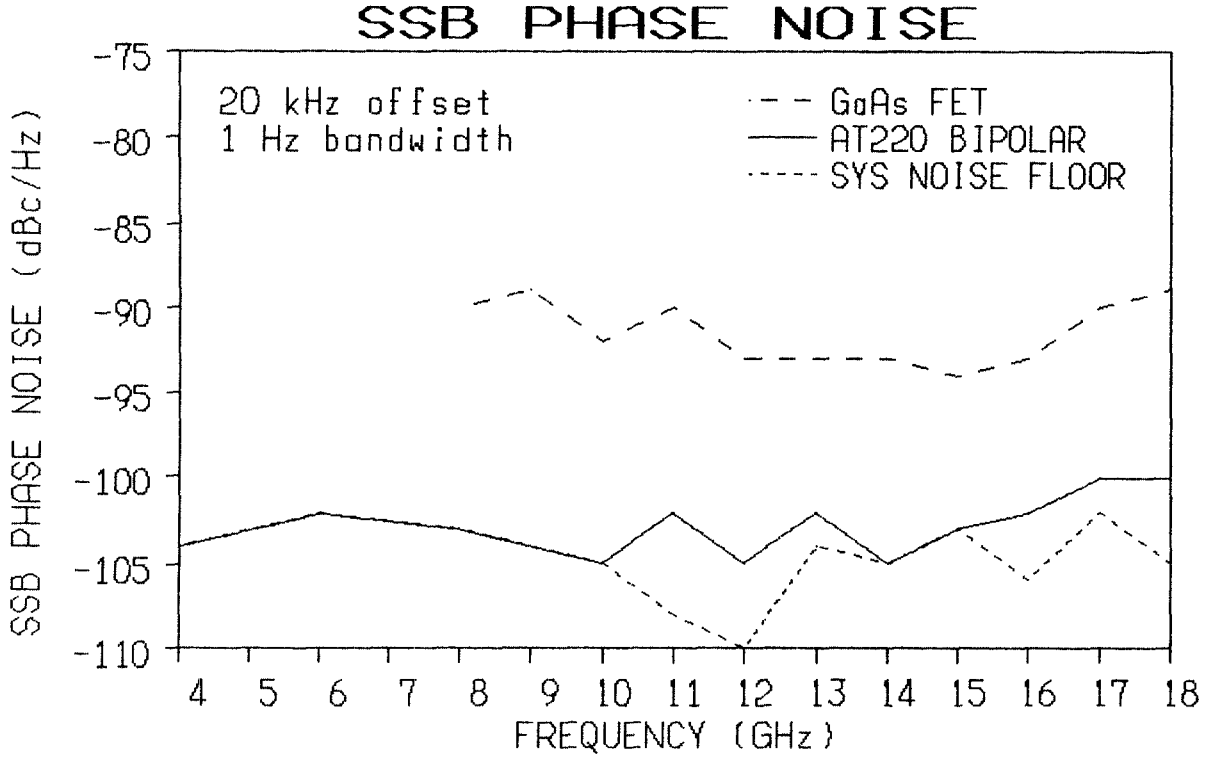



FIG. 6. SSB PHASE NOISE COMPARISON OF SILICON BIPOLAR TRANSISTOR AND TYPICAL GaAs FET BASED YIG-TUNED OSCILLATORS.

## CONCLUSION

Significant improvements in the microwave performance of silicon bipolar transistors have been achieved by aggressive scaling of critical lateral dimensions. Wideband YIG-tuned fundamental oscillators with maximum frequencies above 20 GHz are a practical application which exploits the lower 1/f noise characteristics and wider tuning bandwidth of silicon bipolar transistors versus GaAs FETs.

## ACKNOWLEDGEMENTS

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## REFERENCES

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